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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/884,175	06/19/2001	A. Kent Porterfield	303.760US1	2810

7590 03/21/2007

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EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	**PAPER NUMBER**
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/884,175	PORTERFIELD, A. KENT	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,8-11,13-15,27-29,37,39-41 and 47-59* is/are pending in the application.

4a) Of the above claim(s) *3, 7, 12, 16-26, 30-36, 38, 42-46* is/are withdrawn from consideration.

5)☐ Claim(s) *11,13-15 and 27-29* is/are allowed.

6)☐ Claim(s) *1,2,4-6,8-10,37,39-41 and 47-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the communication filed on 12/04/2006

2. Claims 1-2, 4-6, 8-11, 13-15, 27-29, 37, 39-41, 47-59 are pending for examination.

Claims 3, 7, 12, 16-26, 30-36, 38, are cancelled.

Note: Although, as indicated by the applicant through the communication filed on 12/04/2006 that the applicant has chosen to withdraw claims 42-46 from consideration; however, in the list of claim filed by the applicant, claims 42-46 was not withdraw. Please take the appropriate correction.

3. The text of those sections of Title 35, U.S. code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by PCI Special Interest Group "PCI Bus Power Management Interface Specification" Rev. 11, December 18, 1998 ("Special").

6. As per claim 1, Special discloses an apparatus comprising:

a hardware linked list, the hardware linked list including a plurality of nodes, each of the plurality of nodes including a next node pointer register, wherein each of the plurality of nodes includes a register to specify a capability of the apparatus [Fig. 4 page 23].

Special does not explicitly teach the next node pointer register is writable register or a locking mechanism to conditionally make the next node pointer register of each of plurality of nodes read-only. However, both of this features are deemed to be inherent to the Special system as indicated in page 23 by Special that the capabilities can be in any order wherein the first byte of each register is required to be the ID of that capability and the next byte is a pointer to the next capability in the list. If there are no more entries in the list, the next pointer must be set to 0 to indicate that the end of the linked list has been reached. Therefore, the next node pointer register is inherently writable or else the next node pointer of Special would not able to be set or program to indicate the capabilities of the PCI card. Next, as show in section 3.2.2 of page 25, the next node pointer register of each of plurality of nodes is Read Only. The Special system would not able to lock the next node pointer register of each of plurality of nodes if there is not a locking mechanism to perform the lock condition.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1, 2, 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon U.S. Patent No. 5,925,134 in view of Campbell et al. U.S. Patent No. 5,365,587 ("Campbell").

11. As per claim 1, Solomon discloses an apparatus comprising:

a hardware linked list, the hardware linked list including a plurality of nodes, each of the plurality of nodes including a next node pointer register, wherein each of the plurality of nodes includes a register to specify a capability of the apparatus [col. 7 lines 22-26].

However, Solomon does not explicitly teach the next node pointer register is writable register or a locking mechanism to conditionally make the next node pointer register of each of plurality of nodes read-only.

Campbell teaches another method and system directed to computer system and particularly to the modification of the functional characteristics of a data processing system wherein the system is manufactured having a full set of predetermined functional characteristics and thereafter the control and security logic circuitry may be utilized to selectively enable a subset of those functional characteristics for particular application [col. 7 line 64 to col. 8 line 4].

Specifically, Campbell teaches a hardware list [70 fig. 4], the hardware list including a plurality of node,)], each of the plurality of nodes including a writable register [*inherent – the hardware list may be controlled to enabled and/or disable the specific bit (node) of a functional characteristics of the data processing, permitting the manufacturer to provide a variety of functional characteristic capabilities within a single data processing system* (col. 7 lines 36-45; col. 9 lines 54-65)], wherein each of the plurality of nodes includes a register to specify a capability of the apparatus; and

a locking mechanism [security logic] to conditionally make the node register of each the plurality of nodes read-only [col. 6 lines 61-64].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the hardware linked list of Solomon with the method taught by Campbell. The motivation for doing so would have been to allow the manufacturer to stored a full set of capabilities in a peripheral device and selectively enable a specific subset of capabilities in according to the functional capability of a specific device by modify the next node pointer register in the Solomon hardware linked list without required the manufacturer to store a different set of capabilities for each different peripheral devices; and, secondly, to prevent accidental write or modification to the linked list structure by conditionally make the next node pointer register read-only since an unintended modification to these registers which could change the device configuration/capability resulting in a device failure.

12. As per claim 2, Campbell teaches the locking mechanism comprises a control register [78 fig. 4].

13. As per claim 4, Solomon teaches the apparatus comprises a PCI local bus compliant peripheral device [inherent – col. 7 lines 11-13].

14. As per claim 5, Solomon teaches the apparatus comprise an integrated circuit having a microprocessor bus compatible interface [inherent].

15. Claims 6, 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Special in view of Mitra.

16. As per claim 6, Special teaches a PCI local bus compliant device comprising:

a hardware implemented capabilities list capable of being read-only to higher level software

wherein the hardware implemented capabilities list comprises a plurality of list nodes that each include a writeable next node pointer register [as demonstrated in claim 1].

Special does not specifically teach the hardware implemented capabilities list capable of being modified by low-level software, wherein a modification to the capabilities list by the low level software modifies capabilities available from the PCI local bus compliant device.

Mitra teaches another invention relates to the modification/reprogramming of a PCI peripheral device's configuration information. Specifically, Mitra teaches a hardware implemented capabilities list [col. 1 lines 37-39, col. 2 lines 64-67] capable of being modified by

low level software [col. 4 lines 25-33; col. 9 lines 31-35], and read-only to higher level software[1] [col. 2 lines 52-67], wherein a modification to the capabilities list by the low level software modifies capabilities available from the PCI local bus compliant device [col. 4 lines 61-62; col. 9 lines 32-35].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the hardware implemented capabilities list of Special with ability to be modified by low-level software. The motivation for doing so would have been to provide the system the ability to change or modify the configuration information of a PCI peripheral device as needed.

17. As per claim 9, Mitra does not explicitly teach the hardware implemented capabilities list is writeable by basic input output software and read-only to operating system software.

However, Mitra explicitly teaches that the hardware implemented capabilities list is writeable by any software. Therefore, it is obvious to one of ordinary skill in the art that the generic software of Mitra encompasses the claimed basic input/output software since the particular software does not alter the Mitra system.

and inherently, Mitra teaches the implemented capabilities list is read-only to operating system software.

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[1] As disclose by Mitra, in order to be identified during computer system startup, each PCI peripheral device is capable of reporting certain information referred as configuration information [col. 1 lines 32-39; col. 2 lines 52-59]. The configuration information typically includes parameters for indicating a vendor ID, serial number, base address register, and device capabilities [col. 2 lines 60-64]. Therefore, inherently the configuration information included a capabilities list.

Specifically, Mitra teaches, once the configuration software is able to communicate with the PCI peripheral device, the configuration software can modify the configuration information if necessary. In order to change a particular configuration information value (inherently included the capabilities list), the software stores a new data value in

18. As per claim 10, Mitra teaches the PCI local bus compliant device comprises an integrated circuit that includes the hardware implemented capabilities list [fig. 3].

19. Claims 6-8, 37-41, 47-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (AP) in view of Campbell.

20. As per claim 47, AP teaches a method of initializing a computer peripheral comprising:

writing a list of capabilities to nodes in a hardware linked list within the computer peripheral shortly after the manufacture of the computer peripheral; and

writing to a control register within the computer peripheral to make the nodes read-only.

However, the prior art method of implementing the hardware linked list is inefficient since the list of peripheral device capabilities cannot be modified after the peripheral device is resident in a computer system.

Campbell teaches another method directed to computer system and, particularly, to the modification of the functional characteristics of a data processing system wherein the system is manufactured having a full set of predetermined functional characteristics and thereafter the control and security logic circuitry may be utilized to selectively enable a subset of those functional characteristics for particular application [col. 7 line 64 to col. 8 line 4].

Specifically, Campbell teaches

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the corresponding memory location in the programmable non-volatile memory on the PCI peripheral device [col. 4 lines 25-33; col. 9 lines 32-35].

writing a list of capabilities to nodes in a hardware list [70 fig. 4] within the computer peripheral [50 fig. 4] during initialization of the computer [col. 2 lines 37-62; col. 7 line 65 to col. 8 line 4; col. 9 lines 54-65]; and

writing to a control register [76 fig. 4] within the computer peripheral to make the node read-only [250 fig. 7B; 128 fig. 5].

At the time of the invention was made, it would have been obvious to one or ordinary skill in the art to have modified the hardware linked list of AP with the method taught by Campbell. The motivation for doing so would have been to allow the manufacturer to store a full set of capabilities in a peripheral device and selectively enable a specific subset of those capabilities supported for a particular device; where, in the instant of AP system, the manufacturer only needs to simply modify the node pointer in the hardware linked list to define a different set of capabilities for each different peripheral device. Further more, the method of Campbell would permit the functional capabilities of a peripheral device to be selectively modified without the necessity of physical or mechanical manipulation. Secondly, it would have been obvious to one of ordinary skill in the art to make the nodes read-only to eliminate the possibility of failure due the unintended modification of the capability list as taught by Campbell in col. 6 lines 5-16].

Therefore, it would have been obvious to combine AP with Campbell to obtain the invention as specified in claim 47.

21. As per claim 48, AP teach a capability register and a next node pointer register.

The combine teachings of AP and Campbell teach writing a list of capabilities comprises modifying the next node pointer register [see discussion in claim 47].

22. As per claim 49, Campbell teaches the writing to a control register comprise writing once to a capabilities lock bit, which thereafter is read only [col. 2 line 57].

23. As per claim 50, this feature is inherent to the PCI Bus Power Management Interface Specification.

24. As per claim 51, this feature is inherent to the system of AP modified by Campbell. the system of AP/Campbell would be inoperable if the method is performed by basic input output [col. 6 line 58] was not prior to loading of an operating system.

25. As per claim 52, AP teaches a method of initializing a PCI local bus compliant device comprising:

reading a list of capabilities to nodes in a hardware list within the computer peripheral during initialization of the computer.

AP does not teach reading instructions from a memory device holding basic input output software to modify a link within a capabilities linked list and writing to a control register in the PCI local bus compliant device to make the link read-only.

Campbell teaches reading instruction from a memory device holding basic input output software[col. 2 lines 46-50; 230 fig. 7B];

modifying a node within a capabilities list in the device [col. 2 lines 50-52; 234 fig. 7B]; and

writing to a control register in the device to make the node read-only [col. 7 lines 1-8; 250 fig. 7B; 128 fig. 5].

At the time of the invention was made, it would have been obvious to one of ordinary skill to have modified the PCI local bus compliant device of AP with the method taught by Campbell [see further discussion in claim 47].

26. As per claim 53-54, see discussion in claim 48 and 50.

27. As per claim 52, this feature is inherent to the system of AP modified by Campbell.

28. As per claim 56-57, AP modified by Campbell teaches the method for modifying the next node pointer register in a PCI local bus peripheral to indicate the existence of a capability. Therefore, AP/Campbell teaches a computer readable medium with machine readable instructions to perform the method.

29. As per claim 58-59, inherent to AP apparatus.

30. As per claim 6, AP teaches a PCI local bus compliant device comprising:

a hardware implemented capabilities list capable of being read only to higher level software, where the hardware implemented capabilities list comprises a plurality of list nodes that each include a writeable next node pointer register.

Campbell teaches a hardware implemented capabilities list capable of being modified by low-level software, wherein a modification to the capabilities list by the low level software modified capabilities available from the compliant device [col. 2 lines 46-62].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of AP with the method taught by Campbell [see further discussion in claim 47].

31. As per claim 8, Campbell teach a control register operable to change the capabilities list to read only [128 fig. 5]. Therefore, it is obvious to one of ordinary skill in the art that the combine teaching of AP and Campbell teach a control register being operable to change the writeable next node pointer registers to read-only next node pointer registers.

32. As per claim 37, AP teaches a computer system comprising:

a PCI local bus compliant peripheral devices coupled to a bus; and

a processor coupled to the bus;

wherein the PCI local bus compliant peripheral device includes a capabilities linked list; and

wherein the capabilities linked list comprises a plurality of nodes made up of groups of registers, each node corresponding to one capability.

Campbell teach another computer system. Specifically, Campbell teaches the system includes a capabilities list [70 fig. 4] modifiable by the processor [18 fig. 1], and the system

further includes a writeable control register [68, 78 fig. 4] operable to render the capabilities list read only by the processor.

At the time of the invention was made it would have been obvious to one of ordinary skill in the art to have combine the system of AP with Campbell. [see further discussion in claim 47].

33. As per claim 39, see discussion in claim 47.

34. As per claim 40, inherent to the system of AP modified by Campbell.

35. As per claim 41, this feature is inherent to the PCI Bus Power Management Interface Specification.

Examiner's note:

Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Prior Art not relied upon:

Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Tran